

Lab-3 A Feedback Control System – PLL

Theory

A phase-lock-loop is a typical feedback control system. Figure-1 is the block diagram.

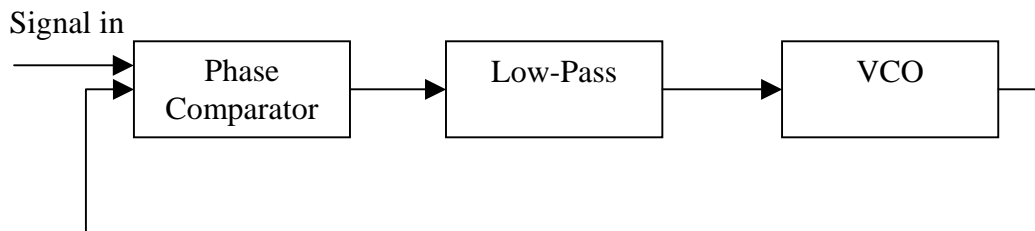


Figure-1 Block diagram of a PLL

1. The Phase Comparator

This circuit outputs the phase difference between the two inputs, signal_in and VCO output. In our experiments, the chip CD4046BC has two phase comparators (PCs). PC 1 is an exclusive OR gate, provides a digital error signal (PC1 output) and maintains 90° phase shifts at the VCO center frequency. PC 2 is an edge-controlled digital memory network. It provides a digital error signal (PC2 output) and a lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input, [1].

2. The Low-Pass Filter

The output of the phase comparator consists of a DC component and a superimposed AC component. We simply use a RC low-pass filter to cancel the undesired AC component.

3. The VCO

The frequency of VCO output signal is proportional to the amplitude of the input signal from the low pass filter. The natural frequency of the VCO is non-zero and is called the center frequency. In our experiment, the CD4046BC has a linear voltage-controlled oscillator (VCO) produces an output signal (VCO output) whose frequency is determined by the voltage of VCO_{in} input, and the C_1 , R_1 and R_2 , [1].

Figure-2 is the connection diagram of CD4046BC.

Figure-3 is the block diagram of CD4046BC.

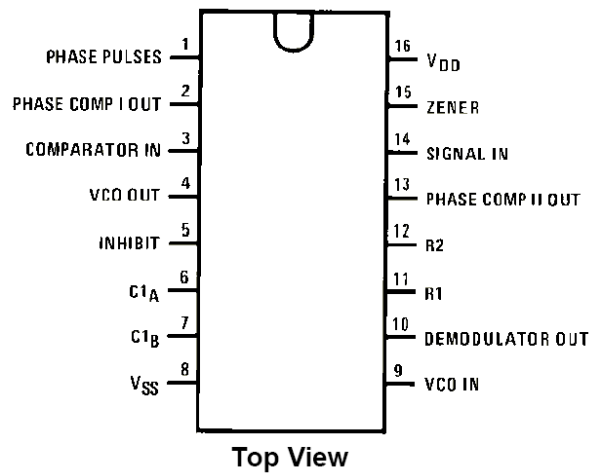


Figure-2 Connection Diagram of CD4046BC

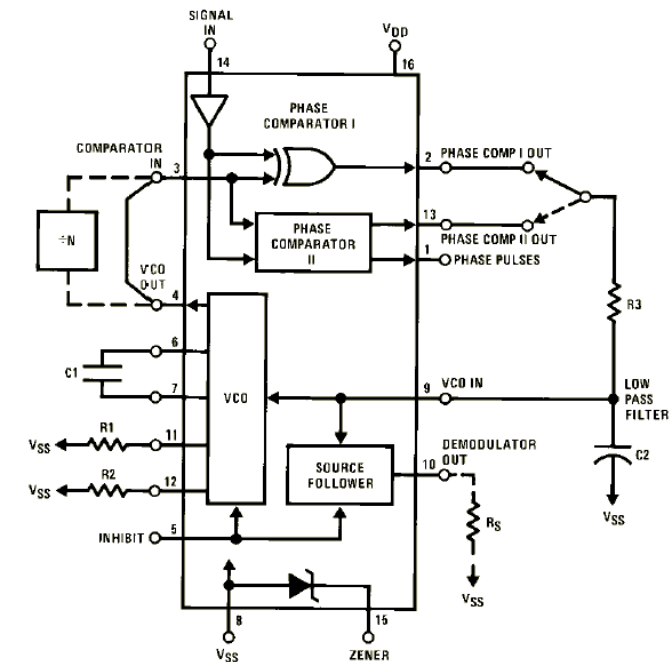


Figure-3 Block Diagram of CD4046BC

Experiments

We use phase comparator II in our experiments. Figure-4 shows the connection diagram.

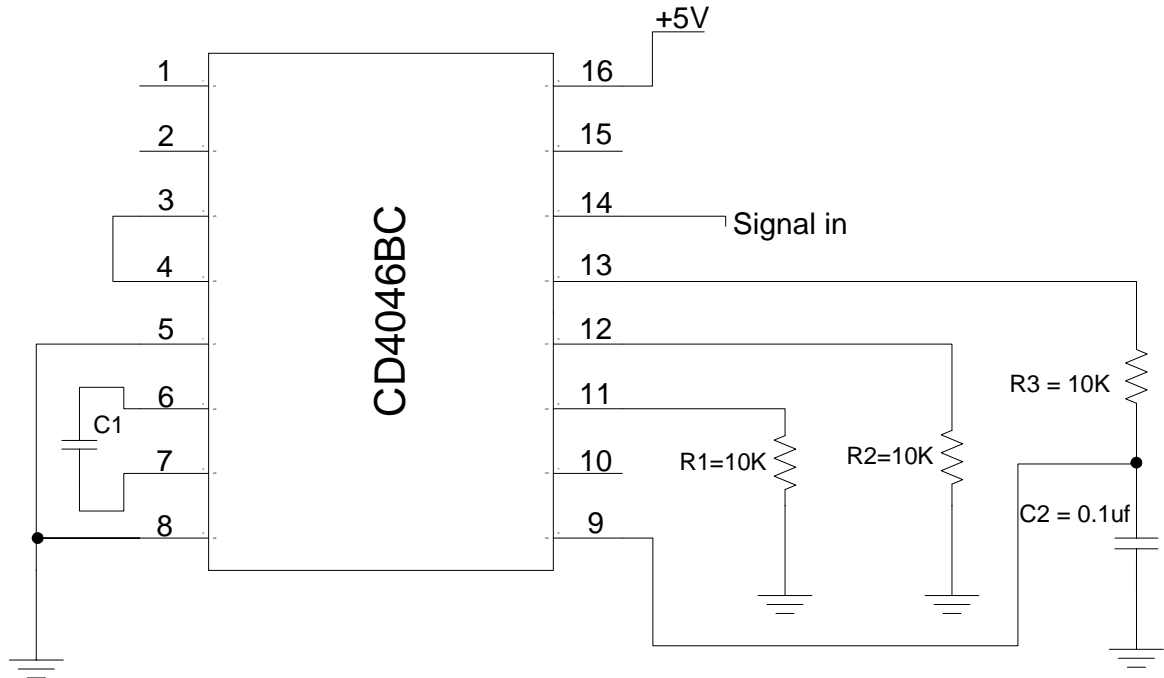


Figure-4 Connection diagram using PCII

1 Measure the f_{min} .

When there is no signal input (connect pin 14 to the ground and VCO_{in} (pin 9) to the ground, PLL system will adjust to the lowest operating frequency, f_{min} . Try to measure f_{min} (at pin 3) with different C_1 while $R_1 = 10K\Omega$ and $R_2 = 10 K\Omega$. Check the Figure 6 in CD4046BC specification [1] to justify your measurement.

Capacitor C_1	Measured F_{min} (Hz)	F_{min} (Hz) in specification
0.01 μF		
0.1 μF		
1 μF		

2 Observe the signals.

Keep $R_1 = 10K\Omega$ and $R_2 = 10 K\Omega$ and $C_1 = 0.1\mu f$. Disconnect pin 9 from the ground. Set the signal generator to square wave mode and 1000Hz. Connect pin 14 to signal generator. Observe and draw the signal wave at pin 14, pin 13, pin 9 and pin 4, respectively.

Signal at pin 14:

Signal at pin 13:

Signal at pin 9:

Signal at pin 4:

3. Measure the operating frequency range.

Use dual channels to observe pin14 and pin4 at the same time. You should be able to observe the VCO output (pin 4) is phase locked to signal_in. Then change the frequency of signal_in and observe when the phase lock is broken. Observe the operating frequency range of signal_in.

Capacitor C_1	Min operating f (Hz)	Max operating f (Hz)
0.01 μ F		
0.1 μ F		
1 μ F		

Change R2 to ∞ and measure again.

Capacitor C_1	Min operating f (Hz)	Max operating f (Hz)
0.01 μ F		
0.1 μ F		
1 μ F		

Disconnect pin 3 and pin 4, can you still observe the phase lock at output pin 4 when you change the frequency of signal_in within the operating range? Why?

Let $C_1 = 0.1\mu\text{F}$. Connect pin3 and pin4 but exchange C_2 and R_3 . Can you observe the phase locked at output pin4 when you change the frequency of signal_in within the operating range? Why?

Reference:

[1] CD4046BC Micropower Phase-Locked Loop specification,
<http://www.fairchildsemi.com/ds/CD/CD4046BC.pdf> .